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SS Results
1 2 (1) ..FAM US20030045074/PN
2 2 (1) ..FAM WO03021640/PN

1 / 2 PLUSPAT - ©QUESTEL-ORBIT - image

PN - WO03021640 A2 20030313 [WO200321640]
PN2 - WO03021640 A3 20030417 [WO200321640]
TI - (A2) METHOD FOR SEMICONDUCTOR GATE DOPING
OTI - (A2) PROCEDE DE DOPAGE DE GRILLE A SEMI-CONDUCTEUR
LA - ENGLISH (ENG)
PA - (A2) ULTRATECH STEPPER INC (US)
PA0 - ULTRATECH STEPPER, INC.; 3050 Zanker Road, San Jose, CA 95134 (US)
PA2 - (A3) ULTRATECH STEPPER INC (US)
IN - (A2) SEIBEL CINDY; TALWAR SOMIT
AP - WOUS0226362 20020815 [2002WO-US26362]
PR - US94181701 20010829 [2001US-0941817]
IC - (A2) H01L-021/00 H01L-021/26 H01L-021/336 H01L-021/425
EC - H01L-021/8238G4
DS - JP; KR; European patent (AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; LU; MC; NL; PT; SE; SK; TR)
DT - Basic
CT - Cited in the search report
US5966605(A)(Cat. Y); US6365476(B1)(Cat. Y,P);US6274488(B1)(Cat. Y);US6077758(
(Cat. Y)
VAN ZANT: 'Microchip fabrication', 2000, MCGRAW-HILL PUBLISHING XP002960(
Fourth edition, pages 331, 403-404, 411(Cat. Y)
STG - (A2) Publ. Of int. Appl. W/out int. Search rep
STG2 - (A3) Subsqu. Publ. Of int. Search report
AB - A method of forming a doped polycrystalline silicon gate in a Metal Oxide Semiconductor "MOS" device. The method includes forming first an insulation layer 114 on a top surface crystalline silicon substrate 106. Next, an amorphous silicon layer 200 is formed on top of contact with the insulation layer 114 and then a dopant is introduced in a top surface layer amorphous silicon layer 200. The top surface 220 of the amorphous silicon layer 200 is irr with a laser beam 230 and the heat of the radiation causes the top surface layer 220 to mel initiates explosive recrystallization "XRC" of the amorphous silicon layer 200. The XRC p transforms the amorphous silicon layer 200 into a polycrystalline silicon gate and distribut dopant homogeneously throughout the polycrystalline gate.
UP - 2003-12

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2 / 2 PLUSPAT - ©QUESTEL-ORBIT

PN - US2003045074 A1 20030306 [US20030045074]
TI - (A1) Method for semiconductor gate doping
IN - (A1) SEIBEL CINDY (US); TALWAR SOMIT (US)
AP - US94181701 20010829 [2001US-0941817]
PR - US94181701 20010829 [2001US-0941817]
IC - (A1) C30B-001/00 H01L-021/3205 H01L-021/336 H01L-021/4763
EC - H01L-021/8238G4
PCL - ORIGINAL (O) : 438486000; CROSS-REFERENCE (X) : 438592000 438308000

STG - (A1) Utility Patent Application published on or after January 2, 2001

AB - A method of forming a doped polycrystalline silicon gate in a Metal Oxide Semiconductor (MOS) device. The method includes forming first an insulation layer on a top surface of a crystalline silicon substrate. Next, an amorphous silicon layer is formed on top of and in c with the insulation layer and then a dopant is introduced in a top surface layer of the amor silicon layer. The top surface of the amorphous silicon layer is irradiated with a laser bean the heat of the radiation causes the top surface layer to melt and initiates explosive recrystallization (XRC) of the amorphous silicon layer. The XRC process transforms the amorphous silicon layer into a polycrystalline silicon gate and distributes the dopant homogeneously throughout the polycrystalline gate.

UP - 2003-12

US 20030045074A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2003/0045074 A1

Seibel et al. (43) Pub. Date: Mar. 6, 2003

(54) METHOD FOR SEMICONDUCTOR GATE DOPING

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(21) Appl. No.: 09/941,817

(22) Filed: Aug. 29, 2001

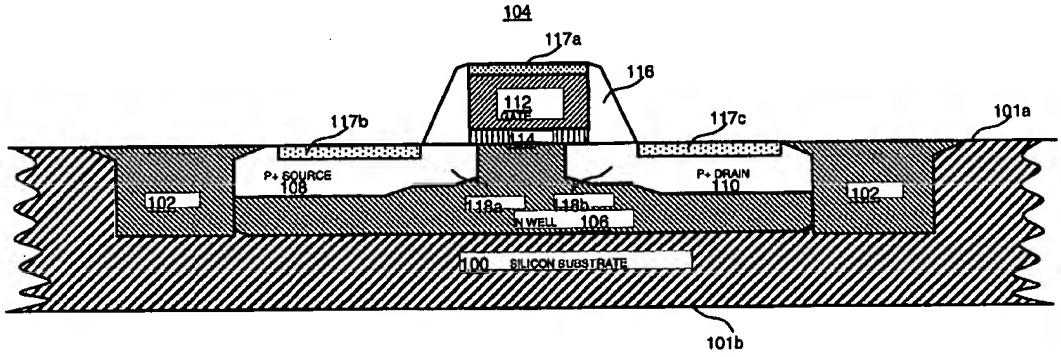
Publication Classification

(51) Int. Cl.[7] H01L 21/336; C30B 1/00; H01L 21/3205; H01L 21/4763

(52) U.S. Cl. 438/486; 438/592; 438/308

(57) ABSTRACT

A method of forming a doped polycrystalline silicon gate in a Metal Oxide Semiconductor (MOS) device. The method includes forming first an insulation layer on a top surface of a crystalline silicon substrate. Next, an amorphous silicon layer is formed on top of and in contact with the insulation layer and then a dopant is introduced in a top surface layer of the amorphous silicon layer. The top surface of the amorphous silicon layer is irradiated with a laser beam and the heat of the radiation causes the top surface layer to melt and initiates explosive recrystallization (XRC) of the amorphous silicon layer. The XRC process transforms the amorphous silicon layer into a polycrystalline silicon gate and distributes the dopant homogeneously throughout the polycrystalline gate.



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Set     Items   Description
S1         82   AU= (SEIBEL C? OR SEIBEL, C? OR TALWAR S? OR TALWAR, S?)
S2     146212   AMORPHOUS
S3    1045224   SILICON? OR SI OR POLYSILICON? OR POLY()SILICON?
S4       3575   LASER?(6N)ANNEAL?
S5         11   S1 AND S2 AND S3 AND S4
S6     288794   XCR OR EXPLOSIVE(2N)RECRYSTALLI? OR CRYSTALLI?
S7         11   S5 AND S6
S8         11   IDPAT (sorted in duplicate/non-duplicate order)
S9         11   IDPAT (primary/non-duplicate records only)
?  show files
File 347:JAPIO Oct 1976-2003/Feb(Updated 030603)
         (c) 2003 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2003/Jun W04
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030626,UT=20030619
         (c) 2003 WIPO/Univentio
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200341
         (c) 2003  Thomson Derwent
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7/TI,PN,AU,AB,AD,PD,AN/1 (Item 1 fr m file: 348)
DIALOG(R)File 348:(c) 2003 European Patent Office. All rts. reserv.

FABRICATION METHOD FOR REDUCED-DIMENSION INTEGRATED CIRCUITS
HERSTELLUNGSVERFAHREN FUR INTEGRIERTE SCHALTKREISE MIT REDUZIERTER DIMENSION
PROCEDE DE FABRICATION DE CIRCUITS INTEGRES AUX DIMENSIONS REDUITES

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PATENT (CC, No, Kind, Date): EP 1012879 A2 000628 (Basic)
EP 1012879 B1 020904
WO 98034268 980806
APPLICATION (CC, No, Date): EP 98909985 980129; WO 98US1942 980129
PRIORITY (CC, No, Date): US 792107 970131

7/TI,PN,AU,AB,AD,PD,AN/2 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2003 WIPO/Univentio. All rts. reserv.

METHOD FOR SEMICONDUCTOR GATE DOPING
PROCEDE DE DOPAGE DE GRILLE A SEMI-CONDUCTEUR

Inventor(s):
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TALWAR Somit , 116 Adrian Place, Los Gatos, CA 95032, US

Patent and Priority Information (Country, Number, Date):
Patent: WO 200321640 A2-A3 20030313 (WO 0321640)
Application: WO 2002US26362 20020815 (PCT/WO US0226362)

English Abstract
A method of forming a doped polycrystalline **silicon** gate in a Metal Oxide Semiconductor "MOS" device. The method includes forming first an insulation layer (114) on a top surface of a **crystalline silicon** substrate (106). Next, an **amorphous silicon** layer (200) is formed on top of and in contact with the insulation layer (114) and then a dopant is introduced in a top surface layer of the **amorphous silicon** layer (200). The top surface (220) of the **amorphous silicon** layer (200) is irradiated with a laser beam (230) and the heat of the radiation causes the top surface layer (220) to melt and initiates **explosive recrystallization** "XRC" of the **amorphous silicon** layer (200). The XRC process transforms the **amorphous silicon** layer (200) into a polycrystalline **silicon** gate and distributes the dopant homogeneously throughout the polycrystalline gate.

French Abstract
L'invention concerne un procede de realisation d'une grille en silicium polycristallin dopee dans un dispositif a semi-conducteur a oxyde metallique (MOS). Ce procede consiste a former d'abord une couche d'isolation sur une surface superieure d'un substrat en silicium cristallin. Par la suite, on forme une couche en silicium amorphe sur la partie superieure de et en contact avec la couche d'isolation, puis on introduit un dopant dans une couche de surface superieure de la couche en silicium amorphe. La surface superieure de la couche en silicium amorphe est soumise a un rayonnement par faisceau laser et la chaleur du rayonnement fait fondre la couche de surface superieure et lance la recristallisation explosive (XRC) de la couche en silicium amorphe. Le processus XRC transforme la couche en silicium amorphe en une grille en

silicium polycristallin et repartit le dopant de maniere homogene a travers la grille en silicium polycristallin.

7/TI,PN,AU,AB,AD,PD,AN/3 (Item 2 from file: 349)

LASER THERMAL PROCESS FOR FABRICATING FIELD-EFFECT TRANSISTORS

PROCEDE THERMIQUE AU LASER PERMETTANT DE FABRIQUER DES TRANSISTORS A EFFET DE CHAMP

Inventor(s):

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Patent and Priority Information (Country, Number, Date):

Patent: WO 200235601 A1 20020502 (WO 0235601)

Application: WO 2001US29120 20010917 (PCT/WO US0129120)

English Abstract

A simplified and cost reduced process for fabricating a field-effect transistor semiconductor device (104) using laser radiation is disclosed. The process includes the step of forming removable first dielectric spacers (116R) on the sides (120a, 120b) of the gate (120). Dopants are implanted into the substrate (100) and the substrate is annealed to form an active deep source (108) and an active deep drain (110). The sidewall spacers are removed, and then a blanket pre-amorphization implant is performed to form source and drain amorphized regions (200a, 200b) that include respective extension regions (118a, 118b) that extend up to the gate. A layer of material (210) is deposited over the source and drain extensions, the layer being opaque to a select wavelength of laser radiation (220). The layer is then irradiated with laser radiation of the select wavelength so as to selectively melt the amorphized source and drain extensions, but not the underlying substrate. This causes dopants in the deep source to diffuse into the molten source extension, and dopants in the deep drain to diffuse into the molten drain extension. Upon recrystallization of the extensions, the layer of material is removed, and the FET device is completed using known processing techniques. The above process eliminates the lithography and ion implantation steps normally required for source and drain extension formation, and thereby reduces the manufacturing costs of field-effect transistors.

French Abstract

L'invention concerne un procede simplifie et a cout reduit permettant de fabriquer un dispositif semi-conducteur de transistor a effet de champ (104) au moyen d'un rayonnement laser. Le procede comprend l'etape consistant a former des premiers espaceurs dielectriques amovibles (116R) sur les cotes (120a, 120b) de la grille (120). Des dopants sont mis en oeuvre dans le substrat (100) qui est recuit de maniere a former une source active profonde (108) et un drain actif profond (110). Les espaceurs de la paroi laterale sont retires et une implantation de couverture de preamorphisation est ensuite executee, en vue de former des regions amorphisees de la source et du drain (200a, 200b), comprenant des regions d'extension respectives (118a, 118b) s'etendant jusqu'a la grille. Une couche de materiau (210) est deposee sur les extensions de la source et du drain, cette couche etant opaque aux fins de selections d'une longueur d'onde de rayonnement laser (220). La couche est ensuite irradiee au moyen d'un rayonnement laser de longueur d'onde selectionnee, de maniere a fondre, de facon selective, les extensions amorphisees de la source et du drain, mais pas le substrat sous-jacent, les dopants dans la source profonde etant contraints de se diffuser dans l'extension fondue de la source et les dopants dans le drain profond etant contraints de se

diffuser dans l'extension fondue du drain. Au moment de la recristallisation des extensions, la couche de materiau est retiree et le dispositif de transistor a effet de champ est acheve au moyen de techniques de traitement connues. Le procede selon l'invention permet d'eliminer les etapes de lithographie et d'implantation ionique, generalement requises pour une formation d'extensions de source et de drain, reduisant ainsi les couts de fabrication de transistors a effet de champ.

7/TI,PN,AU,AB,AD,PD,AN/4 (Item 3 from file: 349)

THERMALLY INDUCED PHASE SWITCH FOR LASER THERMAL PROCESSING
COMMUTATION DE PHASE CAUSEE PAR UN PHENOMENE THERMIQUE, SERVANT AU TRAITEMENT THERMIQUE PAR LASER

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Patent and Priority Information (Country, Number, Date):
Patent: WO 200223279 A1 20020321 (WO 0223279)
Application: WO 2001US42075 20010907 (PCT/WO US0142075)

English Abstract
A method, apparatus and system for controlling the amount of heat transferred to a process region (30) of a workpiece (W) from exposure with a pulse of radiation (10), which may be in the form of a scanning beam (B), using a thermally induced phase switch layer (60). The apparatus of the invention is a film stack (6) having an absorber layer (50) deposited atop the workpiece, such as a **silicon** wafer. A portion of the absorber layer covers the process region. The absorber layer absorbs radiation and converts the absorbed radiation into heat. The phase switch layer is deposited above or below the absorber layer. The phase switch layer may comprise one or more thin film layers, and may include a thermal insulator layer and a phase transition layer. Because they are in close proximity, the portion of the phase switch layer covering the process region has a temperature that is close to the temperature of the process region. The phase of the phase switch layer changes from a first phase (e.g., solid) to a second phase (e.g., liquid or vapor) at a phase transition temperature (T"sub"p). During this phase change, the phase switch layer absorbs heat but does not significantly change temperature. This limits the temperature of the absorber layer and the process region since both are close to the phase change layer.

French Abstract
La presente invention concerne un procede, un appareil et un systeme permettant de commander la quantite de chaleur transferee sur une region de processus (30) d'une piece a travailler (W), a partir d'une exposition a une impulsion de rayonnement (10) qui peut se presenter sous forme d'un faisceau de balayage (B), par utilisation d'une couche de commutation de phase causee par un phenomene thermique (60). L'appareil selon cette invention est un empilement de films (6) qui presente une couche d'absorption (50) deposee au-dessus de la piece a travailler, telle qu'une plaquette en silicium. Une partie de la couche d'absorption recouvre la region de processus. La couche d'absorption absorbe un rayonnement et convertit le rayonnement absorbe en chaleur. La couche de commutation de phase peut comprendre une ou plusieurs couches de film mince et peut presenter une couche d'isolation thermique et une couche de

transition de phase. Du fait de leur proximite, la partie de la couche de commutation de phase qui recouvre la region de processus presente une temperature proche de la temperature de la region de processus. La phase de la couche de commutation de phase varie d'une premiere phase (solide, par exemple) a une seconde phase (liquide ou vapeur, par exemple) a une temperature de transition de phase (T"sub"p). Au cours de cette variation de phase, la couche de commutation de phase absorbe de la chaleur, mais ne change pas sensiblement de temperature, ce qui permet de limiter la temperature de la couche d'absorption et de la region de processus, du fait qu'elles sont toutes les deux proches de la couche de variation de phase.

7/TI,PN,AU,AB,AD,PD,AN/5 (Item 4 from file: 349)

THERMALLY INDUCED REFLECTIVITY SWITCH FOR LASER THERMAL PROCESSING
MODIFICATEUR DE REFLEXIVITE A COMMANDE THERMIQUE POUR TRAITEMENT THERMIQUE AU LASER

Inventor(s):
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WANG Yun, 1411 Chavez Way, San Jose, CA 95131, US,
THOMPSON Michael O, 130 Oakwood Lane, Ithaca, NY 14850, US

Patent and Priority Information (Country, Number, Date):
Patent: WO 200197275 A1 20011220 (WO 0197275)
Application: WO 2001US13977 20010430 (PCT/WO US0113977)

English Abstract
A method, apparatus and system for controlling the amound of heat transferred to a process region (30) of a workpiece (W) from exposure with laser radiation (10) using a thermally induced reflectivity switch layer (60). The apparatus of the invention is a film stack (6) having an absorber layer (50) deposited atop the workpiece, such as a **silicon** wafer. A portion of the absorber layer covers the process region. The absorber layer absorbs laser radiation and converts the absorbed radiation into heat. A reflective switch layer (60) is deposited atop the absorber layer. The reflective switch layer may comprise one or more thin film layers, and preferably includes a thermal insulator layer and a transition layer. The portion of the reflective switch layer covering the process region has a temperature that corresponds to the temperature of the process region. The reflectivity of the reflectivity switch layer changes from a low reflectivity state to a high reflectivity state at a critical temperature so as to limit the amount of radiation absorbed by the absorber layer by reflecting the incident radiation. This, in turn, limits the amount of heat transferred to the process region from the absorber layer.

French Abstract
L'invention concerne un procede, un appareil et un systeme destines a reguler la quantite de chaleur transferee a une zone de traitement (30) d'une piece a travailler (W) lors d'une exposition a un rayonnement laser (10), au moyen d'une couche de modification de reflexivite a commande thermique (60). L'appareil de l'invention est forme d'une pile de films (6) comprenant une couche d'absorption (50) deposee sur la piece de travail, telle qu'une plaquette de **silic ne** . Une partie de la couche d'absorption recouvre la zone de traitement. Cette couche d'absorption absorbe le rayonnement laser et transforme le rayonnement absorbe en chaleur. La couche de modification de reflexivite a commande thermique (60) est deposee sur la couche d'absorption. Cette couche de modification

de reflexivite a commande thermique peut comprendre une ou plusieurs couches de film mince, et comprend de preference une couche d'isolation thermique et une couche de transition. La partie de la couche de modification de reflexivite a commande thermique recouvrant la zone de traitement possede une temperature correspondant a celle de la zone de traitement. La reflexivite de la couche de modification de reflexivite a commande thermique change d'un etat de faible reflexivite a un etat de forte reflexivite a une temperature critique, de facon a limiter la quantite de rayonnement absorbee par la couche d'absorption par reflexion du rayonnement incident. Cela permet de limiter la quantite de chaleur transferee a la zone de traitement par la couche d'absorption.

7/TI,PN,AU,AB,AD,PD,AN/6 (Item 5 from file: 349)

HIGH-SPEED SEMICONDUCTOR TRANSISTOR AND SELECTIVE ABSORPTION PROCESS FOR FORMING SAME

TRANSISTOR A SEMICONDUCTEURS GRANDE VITESSE ET PROCEDE D'ABSORPTION SELECTIVE UTILISE POUR SA FABRICATION

Inventor(s):
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THOMPSON Michael O, 130 Oakwood Lane, Ithaca, NY 14850, US

Patent and Priority Information (Country, Number, Date):
Patent: WO 200180300 A1 20011025 (WO 0180300)
Application: WO 2001US7632 20010308 (PCT/WO US0107632)

English Abstract
A high-speed semiconductor transistor and process for forming same. The process includes forming, in a **Si** substrate (10), spaced apart shallow trench isolations (STIs) (20), and a gate (36) atop the substrate between the STIs. Then, regions (40, 44) of the substrate on either side of the gate are either amorphized and doped, or just doped. In certain embodiments of the invention, extension regions (60, 62 or 60', 62") and deep drain and deep source regions (80, 84 or 80', 84') are formed. In other embodiments, just deep drain and deep source regions (80, 84 or 80', 84') are formed. A conformal layer (106) is then formed atop the substrate, covering the substrate surface (11) and the gate. The conformal layer can serve to absorb light and/or to distribute heat to the underlying structures. Then, at least one of front-side irradiation (110) and back-side irradiation (116) is performed to activate the drain and source regions and, if present, the extensions. **Explosive recrystallization** (124) is one mechanism used to achieve dopant activation. A deep dopant region (120) may be formed deep in the substrate to absorb light and release energy in the form of heat (122) which then activates the doped regions.

French Abstract
L'invention concerne un transistor a semiconducteurs a grande vitesse et son procede de fabrication. Ledit procede consiste a former, dans un substrat **Si** (10), des separations (20) se presentant sous la forme de tranchees superficielles (STI), et une grille (36) au-dessus du substrat entre les STI. Il consiste ensuite a rendre amorphe et a doper, ou seulement a doper les zones du substrat de chaque cote de la grille. Dans certains mode de realisation de l'invention, les zones d'extension (60, 62 ou 60', 62') et les zones profondes du drain ou de la source (80, 84 ou 80', 84') sont formees. Dans d'autres modes de realisation, seules les zones profondes du drain et de la source (80, 84 ou 80', 84') sont formees. Ledit procede consiste ensuite a former une couche de faible

epaisseur sur le substrat, recouvrant la surface (11) du substrat et la grille. Ladite couche de faible epaisseur sert a absorber la lumiere et/ou a repartir la chaleur dans les structures sous-jacentes. Il consiste encore a proceder a une irradiation frontale (110) et a une irradiation arriere (116), de sorte que les zones du drain et de source et, si elles sont presentes, les extensions, soient activees. La recristallisation explosive (124) est un mecanisme utilise pour l'activation des dopants. Une zone de dopant profonde (120) peut etre formee a une profondeur importante dans le substrat, de sorte qu'elle absorbe la lumiere et degage de l'energie sous forme de chaleur (122), qui active ensuite les zones dopees.

7/TI,PN,AU,AB,AD,PD,AN/7 (Item 6 from file: 349)

METHODS FOR DETERMINING WAVELENGTH AND PULSE LENGTH OF RADIANT ENERGY USED FOR ANNEALING

PROCEDES DE DETERMINATION DE LA LONGUEUR D'ONDE ET DE LA DUREE D'IMPULSION D'ENERGIE DE RAYONNEMENT UTILISEE POUR LE RECUIT

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Patent and Priority Information (Country, Number, Date):
Patent: WO 200060655 A1 20001012 (WO 0060655)
Application: WO 2000US5329 20000301 (PCT/WO US0005329)

English Abstract
The invention is directed to methods for determining the wavelength, pulse length, and other features important characteristics of radiant energy used to anneal or to activate the source and drain regions of an integrated transistor device which has been doped through implantation of dopant ions, for example. In general, the radiant energy pulse is determined to have a wavelength from 450 to 900 nanometers, a pulse length of 0.1 to 50 nanoseconds, and an exposure energy dose of from 0.1 to 1.0 Joules per square centimeter.

French Abstract
L'invention concerne des procedes de determination de la longueur d'onde, de la duree d'impulsion et d'autres caracteristiques importantes d'energie de rayonnement utilisee pour le recuit ou l'activation des zones du drain et de la source d'un dispositif transistor integre ayant ete dope par l'implantation, par exemple, d'ions dopants. En general, l'impulsion de l'energie rayonnante presente une longueur d'onde de 450 a 900 nanometres, une duree d'impulsion de 0,1 a 50 nanosecondes et une dose d'exposition de 0,1 a 1,0 Joule par centimetre carre.

7/TI,PN,AU,AB,AD,PD,AN/8 (Item 7 from file: 349)

METHOD FOR FORMING A SILICIDE REGION ON A SILICON BODY

PROCEDE POUR FORMER UNE ZONE DE SILICIURE SUR UN CORPS EN SILICIUM

Inventor(s):
TALWAR Somit ,
VERMA Gaurav,
KRAMER Karl-Joseph,
WEINER Kurt

Patent and Priority Information (Country, Number, Date):

Patent: WO 200017913 A2 20000330 (WO 0017913)
Application: WO 99US11175 19990519 (PCT/WO US9911175)

English Abstract
The invented method produces a silicide region on a **silicon** body that is useful for a variety of purposes, including the reduction of the electrical contact resistance to the **silicon** body or an integrated electronic device formed thereon. The invented method includes a step of producing an **amorphous** region on the **silicon** body using ion implantation, for example, a step of forming a metal layer such as titanium, cobalt or nickel in contact with the **amorphous** region, and a step of irradiating the metal with intense light from a source such as a laser, to cause metal atoms to diffuse into the **amorphous** region to form an alloy region with a silicide composition. In an application of the invented method to the manufacture of a MISFET device, the metal layer is preferably formed with a thickness that is at least sufficient to produce a stoichiometric proportion of metal and **silicon** atoms in the **amorphous** region of the gate of the MISFET device. Importantly, the irradiating step proceeds until the metal overlying the gate alloy region is consumed and the gate alloy region is exposed. The gate alloy region has a higher reflectivity than the metal layer, and thus reduces further thermal loading of the gate alloy region so that silicide growth can be continued in the source and drain regions without adversely impacting the gate of the MISFET device. The invention also includes an integrated MISFET device in which the gate silicide region is greater than the source/drain silicide region.

French Abstract
L'invention concerne un procede permettant de produire une zone de siliciure sur un corps en silicium utilise dans de nombreuses applications, notamment pour reduire la resistance d'un contact electrique vis-a-vis dudit corps en silicium ou d'un dispositif electronique integre a ce dernier. Le procede de cette invention consiste tout d'abord a produire une zone amorphe sur le corps en silicium, par exemple par implantation ionique, puis a former une couche metallique de titane, de cobalt, ou de nickel en contact avec cette zone amorphe, et enfin a soumettre ce metal a un rayonnement lumineux intense provenant d'une source telle qu'un laser, afin d'amener les atomes de metal a se diffuser dans la zone amorphe et a former une zone en alliage renfermant une composition de siliciure. Dans l'une des applications de ce procede permettant de fabriquer un transistor MIS, ladite couche metallique presente de preference une epaisseur suffisante pour produire une proportion stoechiometrique d'atomes de metal et de silicium dans la zone amorphe de ce transistor MIS. L'etape d'irradiation se poursuit jusqu'a ce que le metal recouvrant la zone grille en alliage soit epuise, et que cette zone soit exposee. Cette zone grille en alliage presente par ailleurs une reflectivite superieure a celle de la couche metallique, ce qui permet de reduire d'autant la charge thermique sur cette zone, le siliciure pouvant ainsi continuer a croitre dans les zones source et drain sans pour autant nuire a la grille dudit transistor MIS. Cette invention concerne egalement un transistor MIS integre dans lequel la zone grille de siliciure est plus grande que la zone source/drain de siliciure.

7/TI,PN,AU,AB,AD,PD,AN/9 (Item 8 from file: 349)

GAS IMMERSION LASER ANNEALING METHOD SUITABLE FOR USE IN THE FABRICATION OF REDUCED-DIMENSION INTEGRATED CIRCUITS

PROCEDE DE RECUISSON LASER AVEC IMMERSION DANS UN GAZ PERMETTANT DE FABRIQUER DES CIRCUITS INTEGRES DE DIMENSIONS REDUITES

Inventor(s):
TALWAR Somit ,
WEINER Kurt

Patent and Priority Information (Country, Number, Date):
Patent: WO 200013213 A1 20000309 (WO 0013213)
Application: WO 98US25264 19981125 (PCT/WO US9825264)

English Abstract
A method for fabricating a plurality of shallow-junction metal oxide semiconductor field effect transistors (MOSFETs) which are separated by substantially transparent isolation elements (102). This method includes the amorphization of a selected depth of **silicon** (200) in a **silicon** wafer. A top layer stack of a dielectric and a highly radiation absorbent material are deposited to protect areas of which amorphization is not desired. After the melted **silicon** has cooled and recrystallized, the top layer of highly absorbent material is removed.

French Abstract
Cette invention concerne un procede permettant de fabriquer plusieurs transistors a effet de champ, semi-conducteurs, a base d'oxyde metallique et a jonction superficielle (MOSFET) qui sont separes par des elements isolants globalement transparents (102). Ce procede consiste a rendre amorphe une profondeur predeterminee de silicium (200) dans une plaquette de silicium. Un empilement de couches superieures se composant d'un materiau dielectrique et absorbant fortement les rayonnements est ensuite applique afin de proteger les zones que l'on ne souhaite pas rendre amorphes. Une fois que le silicium fondu s'est refroidi et recristallise, on enleve la couche superieure faite du materiau fortement absorbant.

7/TI,PN,AU,AB,AD,PD,AN/10 (Item 9 from file: 349)

FABRICATION METHOD FOR REDUCED-DIMENSION INTEGRATED CIRCUITS
PROCEDE DE FABRICATION DE CIRCUITS INTEGRES AUX DIMENSIONS REDUITES

Inventor(s):
TALWAR Somit ,
KRAMER Karl-Josef,
VERMA Guarav,
WEINER Kurt

Patent and Priority Information (Country, Number, Date):
Patent: WO 9834268 A2 19980806
Application: WO 98US1942 19980129 (PCT/WO US9801942)

English Abstract
Pre-amorphization of a surface layer of **crystalline silicon** to an ultra-shallow (400) and (402) (e.g., less than 100 nm) depth provides a solution to fabrication problems including (a) high thermal conduction in **crystalline silicon** and (b) shadowing and diffraction-interference effects by an already fabricated gate of a field-effect transistor on incident laser radiation. Such problems, in the past, have prevented prior-art projection gas immersion laser doping from being effectively employed in the fabrication of integrated circuits comprising MOS field-effect transistors employing 100 nm and shallower junction technology.

French Abstract
La pre-amorphisation d'une couche superficielle de silicium cristallin sur une infime epaisseur (p.ex., inferieure a 100 nm) apporte une

solution aux problemes de fabrication au moyen (1) d'une haute conduction thermique dans le silicium cristallin et (2) d'effets d'ombrage et de telescopage des diffractions par une porte deja fabriquee d'un transistor a effet de champ sur rayonnement laser incident. Dans le passe, ces problemes ont empeche d'utiliser efficacement le dopage laser par immersion de gaz de projection, de la technique anterieure, dans la fabrication de circuits integres comprenant des transistors a effet de champ MOS utilisant une technologie de jonction au 100 nm, voire encore moins.

7/TI,PN,AU,AB,AD,PD,AN/11 (Item 10 from file: 349)

METHOD FOR FORMING A SILICIDE REGION ON A SILICON BODY
PROCEDE DE FORMATION D'UNE REGION DE SILICIURE SUR UN CORPS EN SILICIUM

Inventor(s):
TALWAR Somit ,
VERMA Guarav,
KRAMER Karl-Joseph,
WEINER Kurt

Patent and Priority Information (Country, Number, Date):
Patent: WO 9833206 A1 19980730
Application: WO 98US314 19980109 (PCT/WO US9800314)

English Abstract
The method of this invention produces a silicide region on a **silicon** body (1) that is useful for a variety of purposes, including the reduction of the electrical contact resistance to the **silicon** body (1) or an integrated electronic device formed thereon. The invented method includes the steps of producing an **amorphous** region (28) on the **silicon** body (1) using ion implantation (26), for example, forming or positioning a metal (30) such as titanium, cobalt or nickel in contact with the **amorphous** region (28), and irradiating the metal with intense light (31) from a laser source, for example, to cause metal atoms to diffuse into the **amorphous** region (28). The **amorphous** region (28) thus becomes an alloy region with the desired silicide composition. Upon cooling after irradiation, the alloy region becomes partially **crystalline** . To convert the alloy region into a more **crystalline** form, the invented method preferably includes a step of treating the alloy region using rapid thermal annealing, for example. An insulator layer (32) and a conductive lead (34) can subsequently be patterned to establish electrical contact to the silicide region. The low contact resistivity of the silicide region provides the capability to transmit relatively high-frequency electronic signals through the contact region. In a preferred application, the invented method is used to form self-aligned silicide contact regions for the gate, source and drain of a metal-insulator-semiconductor field-effect transistor (MISFET).

French Abstract
Le procede de cette invention produit une region de siliciure sur un corps en silicium (1) utile a diverses fins, notamment pour la reduction de la resistance du contact electrique au corps en silicium (1) ou a un dispositif electronique integre forme sur celui-ci. Le procede de l'invention comprend les etapes de production d'une region amorphe (28) sur le corps en silicium (1) par implantation ionique (26), par exemple, de formation et de positionnement d'un metal (30) tel que le titane, le cobalt ou le nickel en contact avec la region amorphe (28), et d'irradiation du metal avec une lumiere intense (31) tiree d'une source laser, par exemple, afin de provoquer la diffusion des atomes de metal

dans la region amorphe (28). La region amorphe (28) devient ainsi une region d'alliage avec la composition de siliciure voulue. Lors du refroidissement apres irradiation, la region d'alliage devient partiellement cristalline. Afin de convertir la region d'alliage en une forme plus cristalline, le procede de l'invention comprend de preference une etape de traitement de la region d'alliage au moyen d'un recuit thermique rapide, par exemple. Une couche d'isolateur (32) et un fil conducteur (34) peuvent ensuite etre configures pour etablir un contact electrique avec la region en siliciure. La faible resistivite de contact de la region en siliciure permet de transmettre des signaux electroniques de frequence relativement haute a travers la region de contact. Dans une application preferee, le procede de l'invention est utilise pour former des regions de contact en siliciure auto-alignee pour la grille, la source et le drain d'un transistor a effet de champ a semi-conducteur metal-isolant (MISFET).

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     (FILE 'HOME' ENTERED AT 10:33:44 ON 01 JUL 2003)

     FILE 'CAPLUS' ENTERED AT 10:33:56 ON 01 JUL 2003
L1       220920 S AMORPHOUS OR AMORPHITI?
L2       984707 S SILICON? OR SI OR POLYSILICON? OR POLY()SILICON?
L3         5972 S LASER?(6N)ANNEAL?
L4         1063 S L1 AND L2 AND L3
L5          435 S L1(6N)L2(6N)L3
L6          324 S L1(3N)L2(3N)L3
L7         5170 S LASER?(2N)ANNEAL?
L8          996 S L1 AND L2 AND L7
L9          309 S L1(3N)L2(3N)L7
L10      289276 S XCR OR EXPLOSIVE(2N)RECRYSTALLI? OR CRYSTALLI?
L11         131 S L9 AND L10
L12      287911 S DOPING OR DOPED OR DOPANT?
L13          13 S L11 AND L12

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L13 ANSWER 2 OF 13 CAPLUS COPYRIGHT 2003 ACS
AN 2003:21257 CAPLUS
DN 138:81814
TI Semiconductor devices having **crystallized** silicon active regions and fabrication of devices thereof
IN Nakanishi, Takeshi
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2003007716	A2	20030110	JP 2001-182890	20010618
PRAI	JP 2001-182890		20010618		

AB The title fabrication involves (1) depositing an amorphous Si film on an insulative substrate, (2) **doping** a Ni crystg. catalyst material into the **amorphous Si** film, (3) **laser annealing** to **crystallize** the **amorphous Si** film, (4) **doping** into a gate insulator, a gate contact, and the crystd. Si film in the crystd. Si film, (4) forming a Si3N4 interlayer insulator film, (5) high-pressure annealing .ltoreq.20 h at .ltoreq.600.degree. in N2 to provide. The process provides simultaneously gettering of the crystn. catalyst and activating and hydrogenating of the Si film in fabrication of TFTs.

L13 ANSWER 5 OF 13 CAPLUS COPYRIGHT 2003 ACS
AN 1999:233639 CAPLUS
DN 130:260676
TI Laser processing apparatus and process for annealing and **crystallization** of amorphous silicon films for semiconductor devices
IN Ishihara, Hiroaki; Nakashita, Kazuhisa; Ohnuma, Hideto; Tanaka, Nobuhiro; Adachi, Hiroki
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO U.S., 19 pp., Division of U.S. Ser. No. 511,466.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5891764	A	19990406	US 1996-739192	19961030
	JP 06295859	A2	19941021	JP 1992-322737	19921106
	JP 3249606	B2	20020121		
	JP 2001085353	A2	20010330	JP 2000-243484	19921113
	JP 2002118077	A2	20020419	JP 2001-241486	19921113
	US 5643801	A	19970701	US 1995-511466	19950804
PRAI	JP 1992-322737	A	19921106		
	JP 1992-328770	A	19921113		
	US 1993-145587	B3	19931104		
	US 1995-511466	A3	19950804		

AB A laser processing process which comprises laser annealing a Si film 2 .mu.m or less in thickness by irradiating a laser beam 400 nm or less in wavelength and being operated in pulsed mode with a pulse width of 50 ns or more, and preferably, 100 ns or more. A laser processing app. which comprises a laser generation device and a stage for mounting thereon a sample provided sep. from said device, to thereby prevent transfer of vibration attributed to the movement of the stage to the laser generation device and the optical system. A stable laser beam can be obtained to thereby improve productivity.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 13 OF 13 CAPLUS COPYRIGHT 2003 ACS
AN 1980:120384 CAPLUS
DN 92:120384
TI **Laser annealing** of glow discharge **amorphous silicon**
AU Sussmann, R. S.; Harris, A. J.; Ogden, R.
CS Allen Clark Res. Cent., Plessey Res. (Caswell) Ltd., Caswell/Towcester, UK
SO Journal of Non-Crystalline Solids (1980), 35-36(1), 249-54
CODEN: JNCSBJ; ISSN: 0022-3093
DT Journal
LA English
AB Glow-discharge-deposited amorphous Si layers were annealed by a Q-switched ruby laser. The properties of the annealed films were studied as a function of laser energy by electron microscopy, photoluminescence and IR absorption. The changes in structure, H content, bandgap, and d. of states in the annealed layers are discussed. There are considerable similarities between amorphous and annealed materials.

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Set     Items   Description
S1     531284   AMORPHOUS OR AMORPHITI?
S2    2183217   SILICON? OR SI OR POLYSILICON? OR POLY()SILICON?
S3     645482   DOPING OR DOPED OR DOPANT? ?
S4       3473   (POLYCRYSTALL? OR POLY()CRYSTAL?)(3N)GATE? ?
S5    1019146   XCR OR EXPLOSIVE(2N)RECRYSTALLI? OR CRYSTALLI?
S6     102380   (LASER? OR RADIANT(2N)ENERGY)(6N)(ANNEAL? OR THERMAL OR HE-
           AT????)
S7     114678   S1(3N)S2
S8     109858   S1(2N)S2
S9      15662   S3 AND S8 AND S7
S10      6567   S9 AND (LAYER? OR REGION? OR SECTION?)
S11        73   S5 AND S10 AND S6
S12      1877   S5(6N)S6
S13        22   S10 AND S12
S14        20   RD (unique items)
S15        18   S14 AND PY<=2001
?  show files
File   2:INSPEC 1969-2003/Jun W4
         (c) 2003 Institution of Electrical Engineers
File   6:NTIS 1964-2003/Jun W5
         (c) 2003 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2003/Jun W4
         (c) 2003 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2003/Jun W5
         (c) 2003 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/May
         (c) 2003 The HW Wilson Co.
File  94:JICST-EPlus 1985-2003/Jun W4
         (c)2003 Japan Science and Tech Corp(JST)
File  35:Dissertation Abs Online 1861-2003/Jun
         (c) 2003 ProQuest Info&Learning
File  65:Inside Conferences 1993-2003/Jun W5
         (c) 2003 BLDSC all rts. reserv.
File 144:Pascal 1973-2003/Jun W3
         (c) 2003 INIST/CNRS
File 347:JAPIO Oct 1976-2003/Feb(Updated 030603)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200341
         (c) 2003  Thomson Derwent
File 315:ChemEng & Biotec Abs 1970-2003/May
         (c) 2003 DECHEMA
?
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15/9/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

02397447 INSPEC Abstract Number: A85028310, B85010736
Title: Multiple layer sputter deposition and laser annealing of silicon films
Author(s): Anderson, W.W.; MacMillan, H.F.; Katzeff, J.S.; Lopez, M.
Author Affiliation: Lockheed Missiles & Space Co. Inc., Sunnyvale, CA, USA
Conference Title: Energy Beam-Solid Interactions and Transient Thermal Processing Symposium p.241-6
Editor(s): Fan, J.C.C.; Johnson, N.M.
Publisher: North-Holland, New York, NY, USA
Publication Date: 1984 Country of Publication: USA xviii+791 pp.
ISBN: 0 444 00903 5
Conference Sponsor: U.S. Army Res. Office
Conference Date: 14-17 Nov. 1983 Conference Location: Boston, MA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: The formation of single crystal multiple **layers** on silicon substrates with thicknesses in excess of 1 mu m has been demonstrated to be a viable process. Film build-up is via repetitions of the steps (1) pre-deposition chemical cleaning of wafer, (2) magnetron sputter deposition of 0.3 mu m thick **amorphous Si** , (3) interfacial mixing via 190 keV implantation of Si, and (4) film epitaxial **crystallization** via pulsed **laser annealing** . **Doping** has been demonstrated by both (1) P ion implantation and (2) P incorporation from PH/sub 3/ included in the sputter gas ambient. (15 Refs)
Subfile: A B
Descriptors: crystallisation; elemental semiconductors; epitaxial growth; ion implantation; laser beam annealing; semiconductor **doping** ; semiconductor epitaxial **layers** ; semiconductor growth; silicon; sputter deposition
Identifiers: Si films; **doping** ; semiconductor; laser annealing; single crystal multiple **layers** ; chemical cleaning; magnetron sputter deposition; **amorphous Si** ; interfacial mixing; film epitaxial crystallization; P ion implantation; sputter gas ambient
Class Codes: A6170T (Doping and implantation of impurities); A6180B (Ultraviolet, visible and infrared radiation); A6855 (Thin film growth, structure, and epitaxy); A8115C (Deposition by sputtering); B0510D (Epitaxial growth); B2520C (Elemental semiconductors); B2550B (Semiconductor doping)

15/9/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

02063401 INSPEC Abstract Number: A83056948, B83033938
Title: Competition between solid phase epitaxy and random crystallization during CW laser annealing of amorphous Si films
Author(s): Roth, J.A.; Kokorowski, S.A.; Olson, G.L.; Hess, L.D.
Author Affiliation: Hughes Res. Labs., Malibu, CA, USA
Conference Title: Laser and Electron Beam Interactions with Solids. Proceedings of the Materials Research Society Annual Meeting p.169-76
Editor(s): Appleton, B.R.; Celler, G.K.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1982 Country of Publication: Netherlands 832 pp.
ISBN: 0 444 00693 1

Conference Date: 16-19 Nov. 1981 Conference Location: Boston, MA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: The kinetics of amorphous-to-polycrystalline conversion and solid phase epitaxy (SPE) in UHV-deposited Si films have been determined over a wide temperature range by the use of optical reflectivity measurements made during rapid **heating** by a CW Ar **laser** . **Crystallization** rates measured in UHV following film deposition are reported and compared to rates measured in air in order to elucidate the effects of contaminants on the processes. The effects of boron **doping** of nucleation and growth kinetics are also reported. The crystallization rates determined in these studies can be used to predict the volume fraction of polycrystalline material formed during laser-induced SPE growth of thick epitaxial **layers** . (11 Refs)
Subfile: A B
Descriptors: amorphous semiconductors; boron; elemental semiconductors; epitaxial growth; laser beam annealing; nucleation; recrystallisation; reflectivity; semiconductor **doping** ; semiconductor thin films; silicon
Identifiers: UHV deposited film; B **doping** ; elemental semiconductor; solid phase epitaxy; random crystallization; CW laser annealing; **amorphous Si** films; optical reflectivity; contaminants; nucleation; growth kinetics; volume fraction of polycrystalline material; thick epitaxial **layers**
Class Codes: A6180B (Ultraviolet, visible and infrared radiation); A6855 (Thin film growth, structure, and epitaxy); B2520C (Elemental semiconductors); B2520F (Amorphous and glassy semiconductors); B2550B (Semiconductor doping); B4360 (Laser applications)

15/9/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

01495911 INSPEC Abstract Number: B80018977
Title: Fabrication of ultra-thin, high quality, single-crystal silicon membranes
Author(s): Petersen, K.E.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.22, no.5 p.2080-1
Publication Date: Oct. 1979 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: It is proposed that a heavily **doped** n/sup +/ substrate should be coated by chemical vapor deposition with a **polysilicon** or **amorphous silicon** film to the desired thickness, with the desired **dopant** level (films <or approximately=1000 A are readily achievable). Next the wafer is **laser annealed** to **crystallize** the top silicon **layer** with the same crystallographic orientation as the substrate. Since the laser anneal step is so rapid and localized at the surface, very little additional diffusion of **dopant** will occur-in contrast to epitaxial depositions. Then the substrate can be etched away either electrochemically or by a **dopant** selective etch, leaving a very thin, single-crystal membrane of high quality, with any desired **dopant** level. Membranes fabricated by this method will be much thinner than with any other technique; thickness and uniformity will also be much easier to control. (0 Refs)
Subfile: B
Descriptors: CVD coatings; etching; membranes; semiconductor **doping** ; silicon
Identifiers: crystallographic orientation; laser anneal; **dopant**

selective etch; high quality; single crystal Si membranes; chemical vapour deposition; ultrathin membranes
Class Codes: B0520F (Vapour deposition); B2520C (Elemental semiconductors); B2550 (Semiconductor device technology)

15/9/12 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05852361 **Image available**
THIN FILM TRANSISTOR AND ITS MANUFACTURE

PUB. NO.: 10-135461 [JP 10135461 A]
PUBLISHED: May 22, 1998 (**19980522**)
INVENTOR(s): HINO TAKASHI
APPLICANT(s): TOSHIBA ELECTRON ENG CORP [486766] (A Japanese Company or Corporation), JP (Japan)
TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-285029 [JP 96285029]
FILED: October 28, 1996 (19961028)
INTL CLASS: [6] H01L-029/786; G02F-001/136; H01L-021/336
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 29.2 (PRECISION INSTRUMENTS -- Optical Equipment)
JAPIO KEYWORD:R002 (LASERS); R011 (LIQUID CRYSTALS); R096 (ELECTRONIC MATERIALS -- Glass Conductors); R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)

ABSTRACT
PROBLEM TO BE SOLVED: To realize cost down by reducing the number of PEPs of a process.

SOLUTION: An **amorphous silicon** film in which n+ is **doped** is formed on a glass substrate 11, n-type high concentration **regions** 12 are formed, an i-type **amorphous silicon** film is deposited and is **crystallized** by **laser annealing**, elements are isolated, and aim n-type active **layer** 13 and a p-type active **layer** 14 are formed. Subsequently, a gate electrode 16a for a p-type transistor is formed on the active **layer** 13 by forming and etching a gate insulating film 15 and depositing a material forming a gate electrode on the film 15. A part on the active **layer** 14 is left as a mask for an MoW 16b, a p-type high concentration **region** is formed in the active **layer** 14 by implanting high concentration impurities, and a gate electrode for an n-type transistor is formed by etching. A low concentration **region** is formed in the active **layer** 14 by implanting low concentration impurities, an interlayer insulating film is formed, contact holes are opened in the interlayer insulating film, a metal film is deposited on the contact holes, and a signal line is formed by etching.

15/9/13 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05487812 **Image available**
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 09-102612 [JP 9102612 A]
PUBLISHED: April 15, 1997 (**19970415**)

INVENTOR(s): HINO TAKASHI
APPLICANT(s): TOSHIBA ELECTRON ENG CORP [486766] (A Japanese Company or Corporation), JP (Japan)
TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-260385 [JP 95260385]
FILED: October 06, 1995 (19951006)
INTL CLASS: [6] H01L-029/786; H01L-021/336; G02F-001/136; H01L-021/265; H01L-021/268
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 29.2 (PRECISION INSTRUMENTS -- Optical Equipment)
JAPIO KEYWORD: R002 (LASERS); R096 (ELECTRONIC MATERIALS -- Glass Conductors); R100 (ELECTRONIC MATERIALS -- Ion Implantation)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method of manufacturing a semiconductor device wherein the dissolving of a problem of uniformity of film quality of a polycrystalline silicon film in a low temperature process, the improvement of annihilation ratio of crystal defect, the improvement of characteristics of a thin film transistor, and the uniforming of characteristics in a substrate are possible.

SOLUTION: An **amorphous silicon** film 12 is **doped** with fluorine before crystallization of a polycrystalline silicon film 13 not through an oxide film, before an element isolation process, by combining **laser annealing** with fluorine **doping** . After that, **crystallization** of the **amorphous silicon** film 12 and activation of fluorine are simultaneously performed by laser annealing. Thereby crystal defect in an active **layer** film 14 is annihilated, and characteristics of film quality is improved as a whole. Hence, the problem of uniformity of film quality of the active **layer** film 14 is dissolved, and excellent characteristics of a polycrystalline silicon thin film transistor in a low temperature process can be obtained in a large-sized substrate without irregularity.

15/9/14 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013941059 **Image available**
WPI Acc No: 2001-425273/ **200145**
XRAM Acc No: C01-128650
XRPX Acc No: N01-315522
Top gate amorphous silicon thin film transistor production for flat panel display comprises laser annealing areas not shielded by gate conductor to form polysilicon portions with diffused impurities
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG)
Inventor: BATTERSBY S J
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200139265	A1	20010531	WO 2000EP10904	A	20001102	200145	B
EP 1147551	A1	20011024	EP 2000983109	A	20001102	200171	
			WO 2000EP10904	A	20001102		
KR 2001093264	A	20011027	KR 2001708995	A	20010716	200223	
JP 2003515928	W	20030507	WO 2000EP10904	A	20001102	200331	
			JP 2001540835	A	20001102		

Priority Applications (No Type Date): GB 9927287 A 19991119
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
WO 200139265 A1 E 21 H01L-021/336
Designated States (National): JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
EP 1147551 A1 E H01L-021/336 Based on patent WO 200139265
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
KR 2001093264 A H01L-029/786
JP 2003515928 W 19 H01L-021/336 Based on patent WO 200139265

Abstract (Basic): WO 200139265 A1

NOVELTY - **Doped** silicon source and drain **regions** (6a,8a) in a thin-film transistor underlie an **amorphous silicon layer** (12) so that **laser annealing** then results in full **crystallization** of the **amorphous silicon layer** .

DETAILED DESCRIPTION - A top gate thin-film transistor is produced by forming **doped** silicon source and drain **regions** (6a,8a) on an insulating substrate, carrying out plasma treatment, forming an **amorphous silicon layer** (12) followed by an insulated gate structure (14,16) and laser annealing areas not shielded by gate conductor to form polysilicon portions having diffused impurities.

An INDEPENDENT CLAIM is also included for a transistor formed as above.

USE - In forming thin-film transistors (claimed)

ADVANTAGE - The **amorphous silicon layer** is fully crystallized, reducing resistance and preventing peeling from the electrodes.

DESCRIPTION OF DRAWING(S) - The figure shows a cross- **section** of the transistor.

Source and drain **regions** (6a,8a)

Amorphous silicon layer (12)

Insulated gate structure (14,16)

pp; 21 DwgNo 2/3

Title Terms: TOP; GATE; AMORPHOUS; SILICON; THIN; FILM; TRANSISTOR; PRODUCE ; FLAT; PANEL; DISPLAY; COMPRISE; LASER; ANNEAL; AREA; SHIELD; GATE; CONDUCTOR; FORM; PORTION; DIFFUSION; IMPURE
Derwent Class: L03; P81; U11; U12; U14
International Patent Class (Main): H01L-021/336; H01L-029/786
International Patent Class (Additional): G02F-001/1343; G02F-001/136; G02F-001/1368; H01L-021/20; H01L-021/225; H01L-021/268
File Segment: CPI; EPI; EngPI
Manual Codes (CPI/A-N): L03-G04A; L03-G05; L04-C10B; L04-E01
Manual Codes (EPI/S-X): U11-C03D; U11-C03J1; U11-C18A1; U12-B03A; U12-Q; U14-K01A2B

15/9/15 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013841375 **Image available**
WPI Acc No: 2001-325588/ **200134**
XRAM Acc No: C03-036098
XRPX Acc No: N03-112258
Polysilicon thin film transistor manufacturing method for liquid crystal display, dynamic random access memory, involves crystallizing amorphous silicon layer **formed n substrate by sequential lateral solidification laser annealing**
Patent Assignee: LG PHILIPS LCD CO LTD (GLDS)

Inventor: CHUNG Y H; JUNG Y H
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2000074373	A	20001215	KR 9918275	A	19990520	200134	B
US 6475872	B1	20021105	US 2000573350	A	20000519	200314	
KR 333275	B	20020424	KR 9918275	A	19990520	200270	

Priority Applications (No Type Date): KR 9918275 A 19990520
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2000074373	A			G02F-001/136	
US 6475872	B1		7	H01L-021/20	
KR 333275	B			G02F-001/136	Previous Publ. patent KR 2000074373

Abstract (Basic): US 6475872 B1

NOVELTY - **Amorphous silicon layer** formed on substrate (210) is **crystallized** using sequential lateral solidification (SLS) **laser annealing** technique to form polysilicon **layer** . Gate insulating **layer** (240) and gate electrode (250) are formed on polysilicon **layer** . Polysilicon **layer** is ion- doped to form source and drain **regions** (230b, 230c).

DETAILED DESCRIPTION - Gate electrode and source and drain **regions** are activated using SLS laser annealing technique.

USE - The method is used for manufacturing polysilicon thin film transistor (TFT) used in high density static random access memory (SRAM) for load pull-up device. The TFT is also used as switching element and peripheral drive circuit in large-area active matrix liquid crystal display (LCD).

ADVANTAGE - By **crystallizing** the **amorphous silicon layer** using SLS **laser annealing** technique, polysilicon **layer** with dense and uniform-sized grains is obtained. Hence the electric characteristics of the transistor are improved and low-resistant gate electrode is obtained.

DESCRIPTION OF DRAWING(S) - The figure shows a cross- **sectional** view illustrating the TFT manufacturing method.

Substrate (210)
Source and drain **regions** (230b, 230c)
Gate insulating **layer** (240)
Gate electrode (250)
pp; 7 DwgNo 3C/3

Title Terms: THIN; FILM; TRANSISTOR; MANUFACTURE; METHOD; LIQUID; CRYSTAL; DISPLAY; DYNAMIC; RANDOM; ACCESS; MEMORY; CRYSTAL; AMORPHOUS; SILICON; **LAYER** ; FORMING; SUBSTRATE; SEQUENCE; LATERAL; SOLIDIFICATION; LASER; ANNEAL
Derwent Class: L03; P81; U11; U12; U13; U14
International Patent Class (Main): G02F-001/136; H01L-021/20
File Segment: CPI; EPI; EngPI
Manual Codes (CPI/A-N): L03-G04A; L03-G05B; L04-C02B; L04-C03; L04-C10B; L04-C11C1; L04-C12; L04-C16A; L04-E01E
Manual Codes (EPI/S-X): U11-C03D; U11-C03J2A; U11-C05F5; U11-C18A1; U12-B03A; U12-Q; U13-C04B1B; U14-A03B1; U14-H01A; U14-K01A2B

15/9/16 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013770820 **Image available**
WPI Acc No: 2001-255031/ **200126**

Related WPI Acc No: 2001-189746
XRAM Acc No: C01-083154
XRPX Acc No: N01-195679
Manufacture of thin film transistor by depositing amorphous silicon **on substrate and patterning t form active** layer , **heavily** doping **impurities in active** layer , **and converting active** layer **of** amorphous silicon **to** polysilicon
Patent Assignee: LG PHILIPS LCD CO LTD (GLDS)
Inventor: LEE J H; LEE S G; LEE S; YI J
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2000061176	A	20001016	KR 9910051	A	19990324	200126	B
US 6207481	B1	20010327	US 99458468	A	19991209	200129	
KR 317622	B	20011222	KR 9910051	A	19990324	200250	

Priority Applications (No Type Date): KR 9910051 A 19990324
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2000061176	A			H01L-029/786	
US 6207481	B1		19	H01L-029/786	
KR 317622	B			H01L-029/786	Previous Publ. patent KR 2000061176

Abstract (Basic): US 6207481 B1

NOVELTY - A thin film transistor is manufactured by depositing **amorphous silicon** on substrate and patterning the deposited **amorphous silicon** to form an active **layer** , heavily **doping** impurities in the active **layer** using gate electrode as mask to form source and drain **region** in the active **layer** , and converting active **layer** from **amorphous silicon** to **polysilicon** through metal induced crystallization process.

DETAILED DESCRIPTION - Manufacture of thin film transistor involves depositing **amorphous silicon** on a substrate and patterning to form an active **layer** (218). A block **layer** is formed centrally located on the active **layer** to function as mask during an impurity **doping** process so that a channel **region** is defined in an approximately central portion in the active **layer** . An exposed surface of the active **layer** is silicidized to form a crystallization seed **layer** (224), and the block **layer** is then removed. A gate insulating **layer** (226) is formed on the substrate to cover the active **layer** and the crystallization seed **layer** . A gate electrode (228) is defined on the gate insulating **layer** so that the gate electrode is located on a portion which corresponds to the channel **region** of the active **layer** , with the gate electrode overlapping with a portion of the crystallization seed **layer** . The active **layer** is heavily **doped** with impurities using the gate electrode as a mask to form source and drain **regions** (230, 231) in the active **layer** from **amorphous silicon** to **polysilicon** through a metal induced lateral crystallization process caused by the crystallization seed **layer** .

USE - For manufacturing a thin film transistor used as switching devices for a pixel block and driving devices for a driver circuit block in an active matrix type liquid crystal display.

ADVANTAGE - The active **layer** is formed of polysilicon providing crystals, which are uniform in size, making the electrical properties of the resulting transistor uniform. The source and drain **regions** are not in direct contact with first and second interconnecting **layers** so that oxidation of the source and drain **regions** is avoided to prevent the contact resistance from increasing.

DESCRIPTION OF DRAWING(S) - The figure shows a cross- **sectional** view of a process for manufacturing the thin film transistor.

Active **layer** (218)
Crystallization seed **layer** (224)
Gate insulating **layer** (226)
Gate electrode (228)
Source and drain **regions** (230, 231)
pp; 19 DwgNo 6E/7
Technology Focus:
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The method further comprises forming a buffer **layer** on the substrate. The crystallization seed **layer** is formed by depositing a high melting point metal, and silicidizing a boundary by a spontaneous reaction of the active **layer** and the deposited high melting point metal. The impurities inside the active **layer** are activated to **crystallize** the active **layer** by using **laser** radiation or by **heat** treatment at 400-600degreesC for 1-3 hours.
INORGANIC CHEMISTRY - Preferred Components: The buffer **layer** is silicon oxide or silicon nitride. The high melting point metal can be titanium, chrome, nickel, molybdenum, tantalum, cobalt, platinum, or tungsten. The block **layer** is made of silicon nitride or silicon oxide having a different etching selection ratio than the buffer **layer** .
Title Terms: MANUFACTURE; THIN; FILM; TRANSISTOR; DEPOSIT; AMORPHOUS; SILICON; SUBSTRATE; PATTERN; FORM; ACTIVE; **LAYER** ; HEAVY; DOPE; IMPURE; ACTIVE; **LAYER** ; CONVERT; ACTIVE; **LAYER** ; AMORPHOUS; SILICON
Derwent Class: L03; U11; U12; U14
International Patent Class (Main): H01L-029/786
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C02; L04-C03; L04-C04; L04-C06; L04-C10B; L04-C10H
Manual Codes (EPI/S-X): U11-C01J2; U11-C03D; U11-C03J1; U11-C18A1; U12-B03A ; U12-Q; U14-K01A2B

15/9/18 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010049567 **Image available**
WPI Acc No: 1994-317278/ **199439**
XRAM Acc No: C94-144602
XRPX Acc No: N94-249094
Solid state imaging device and manufacture - has MOS structure and non-single crystal silicon
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME); TDK CORP (DENK)
Inventor: ARAI M; CODAMA M; INUSHIMA T; KOBORI I; SAKAMOTO N; SUGIURA K; TAKAYAMA I; YAMAUCHI Y
Number of Countries: 018 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9422173	A1	19940929	WO 94JP452	A	19940322	199439	B
JP 6342899	A	19941213	JP 9363789	A	19930323	199509	
EP 642179	A1	19950308	EP 94910053	A	19940322	199514	
			WO 94JP452	A	19940322		
JP 7142694	A	19950602	JP 93314135	A	19931119	199531	
EP 642179	A4	19950830	EP 94910053	A	19940000	199618	
US 5574293	A	19961112	WO 94JP452	A	19940322	199651	
			US 94343492	A	19941122		
US 5591988	A	19970107	WO 94JP452	A	19940322	199708	
			US 94343492	A	19941122		
			US 95477104	A	19950607		
EP 642179	B1	19990203	EP 94910053	A	19940322	199910	

			WO 94JP452	A	19940322	
DE 69416363	E	19990318	DE 616363	A	19940322	199917
			EP 94910053	A	19940322	
			WO 94JP452	A	19940322	

Priority Applications (No Type Date): JP 93314135 A 19931119; JP 9363789 A 19930323

Cited Patents: CH 596671; DE 2541117; EP 165764; FR 2284984; JP 2181419; JP 3009562; JP 323671; JP 5154790; JP 61007663; JP 63029924; NL 7510655; US 4598305; 2.Jnl.Ref; JP 2210877

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9422173	A1			H01L-031/113	
Designated States (National): US					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
JP 6342899	A		9	H01L-027/146	
EP 642179	A1	E	26	H01L-031/113	Based on patent WO 9422173
Designated States (Regional): DE FR GB NL					
JP 7142694	A		8	H01L-027/146	
US 5574293	A		17	H01L-031/062	Based on patent WO 9422173
US 5591988	A		18	H01L-029/04	Div ex application WO 94JP452 Div ex application US 94343492
EP 642179	B1	E		H01L-031/113	Based on patent WO 9422173
Designated States (Regional): DE FR GB NL					
DE 69416363	E			H01L-031/113	Based on patent EP 642179 Based on patent WO 9422173
EP 642179	A4			H01L-031/113	

Abstract (Basic): WO 9422173 A

An active **layer** (3') consisting of non-single-crystal silicon is formed by a thin-film technology on a substrate (1) coated with an insulation **layer** (2), and a gate electrode **layer** (5') is partially disposed on the active **layer** (3') through a gate insulation **layer** (4'). An imaging device having a MOS structure can be obtained by introducing P- or N-type impurity into the active **layer** (3'). A bias voltage is applied to the gate electrode in such a manner that forward current flows between source and drain. When input light is applied to the active **layer** between the source and the drain through the gate electrode or the substrate, an electric output corresponding to the input light is obtained from the source or the drain. MOS transistors are provided on the substrate (1) to form switching devices and shift registers, which are necessary for the operation of the imaging device. The active **layer** (3') can be obtained by **crystallising** an **amorphous silicon layer** by **laser annealing** or high temperature **annealing** with hydrogenation, and a trap density less than 5 x 10 power(11)/cm2 is realised.

ADVANTAGE - The light response time of the imaging device is several hundreds of microseconds (micro-secs.), that is, 10 times or higher than the response of a conventional photosensor using **amorphous silicon** .

Dwg.1/12

Abstract (Equivalent): US 5574293 A

A method for producing a solid state image sensor having a thin film transistor comprising the steps of; providing a silicon oxide **layer** on a substrate, providing an **amorphous silicon layer** on the silicon oxide **layer** by using disilane gas, providing a crystallized non-single crystal silicon **layer** by annealing the **amorphous silicon layer** by illuminating the **amorphous silicon layer** with a laser beam of short pulse width so that the trap density

of the silicon **layer** is less than 5multiplied by1011/cm2, providing an island of the crystallized non-single crystal silicon **layer** , the island being an active **layer** , providing a gate insulation **layer** and a gate electrode **layer** on the active **layer** , and **doping** impurities in the active **layer** to provide a source **regi n** and a drain **region** .

Dwg.0/12

US 5591988 A

A solid state image sensor comprising; a substrate having insulation surface, an active **layer** of non-single crystal silicon **layer** provided on the insulation surface, having at least a source **region** and a drain **region** , a gate electrode **layer** provided on light receiving **region** between the source **region** and the drain **region** on the active **layer** through a gate insulation **layer** , a source electrode **layer** and a drain electrode **layer** each provided on the source **region** and the drain **region** , respectively, trap density of the active **layer** being less than 5 x 1011/cm2, the gate electrode **layer** being provided a predetermined bias potential, and electrical output of current between the source electrode **layer** and the drain electrode **layer** being provided depending upon input light which illuminates the light receiving **region** on the active **layer** .

Dwg.1/12

Title Terms: SOLID; STATE; IMAGE; DEVICE; MANUFACTURE; MOS; STRUCTURE; NON; SINGLE; CRYSTAL; SILICON

Derwent Class: L03; U11; U13; U14

International Patent Class (Main): H01L-027/146; H01L-029/04; H01L-031/062; H01L-031/113

International Patent Class (Additional): H01L-029/784; H01L-029/786; H01L-031/036; H01L-031/0376; H01L-031/10; H01L-031/20

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C02; L04-C11C; L04-E01B; L04-E05

Manual Codes (EPI/S-X): U11-C18A1; U13-A01B; U14-H01B

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